ISSN: 2582 - 6379
Orange Publications
International Journal for Interdisciplinary Sciences and Engineering Applications
IJISEA - An International Peer- Reviewed Journal
2021,June, Volume 2 Issue 2
www.ijisea.org

# Design and Power Analysis of Flip-Flops Using Reversible Logic and Transmission Gate Logic

[1]Hanish Sai Prathi, [2]B.Vinay, [3]A.Sowjanya [4]Emani Ram Naga Kumar,
[5]G.Pooja Sree, [6]A.Mounika Rani, [7]B.Raji

[1]B.Tech, Department of ECE, DMSSVH College of Engineering, Machilipatnam,AP,India
[2]Assistant Professor, Department of ECE, D.M.S.S.V.H College of Engineering, Machilipatnam,AP,India
[34567] B.Tech, Department of ECE, DMSSVH College of Engineering, Machilipatnam,AP,India

hanishprathi@gmail.com , vinaybandekolla@gmail.com ,
sowjanya.anumakonda@gmail.com , ramkumaremani955@gmail.com ,
pooja.gudiseva@gmail.com , mounikarani172@gmail.com , bandiraji26@gmail.com

## ABSTRACT

In the past few years the demand for the lower power devices has increased drastically. By the usage of reversible logic circuits and transmission gate logic, the problem of power dissipation can be reduced. All the operations in the reversible circuits are carried out in a backward manner, which allows reproducing the inputs from the outputs and consumes zero power. Flip-flops are the basic storage elements in any sequential logic circuits. The reversible logic gates are used to implement the flip-flop with the reduced latency and low power dissipation. The transmission gate logic is used to synthesize the flip-flops with the reduced number of gates when compared to the existing model.

**Key Words:** Flip-Flops, Transmission Gate Logic, Reversible Logic, Power Dissipation

## I.INTRODUCTION

Designing of a complex digital system which dissipates low power is a competitive topic in the research field of hardware design. Heat dissipation in the circuit has become the critical limiting factor. Rolf Landauer introduced that losing of bit in circuits causes the smallest amount of heat in computation and the theoretical limit of energy dissipation for losing of one bit computation is ktln2 [5]. Now a days we are experiencing the problem of one's mobile battery dying, or low battery problems for our electronic devices. Almost all the electronic devices we are using are portable. The problem with these electronic devices is that there is not always a power source available, and so the demand for devices that use less power is quickly growing. The generated heat from the electronic circuits can be problematic for larger circuits. Bennett showed that circuits must be built using reversible logic gates only to avoid the heat dissipation.

## II.PROPOSED WORK

The proposed method uses reversible logic and transmission gate logic. The main use of this reversible logic is that there is one to one correspondence between inputs and outputs. Reversible logic is also considered as alternative form of traditional irreversible computing as reversible does not erase or lose any information. As a result, reversible logic has a theoretical potential to dissipate no energy.
Along with the reversible logic, transmission gate logic will also help in reducing the number of gates used to design the sequential circuits. In electronics, pass transistor describes several logic families used in the design of integrated circuits. By using this transmission gate logic we can reduces the count of transistors required to make different logic gates, by avoiding redundant transistors.

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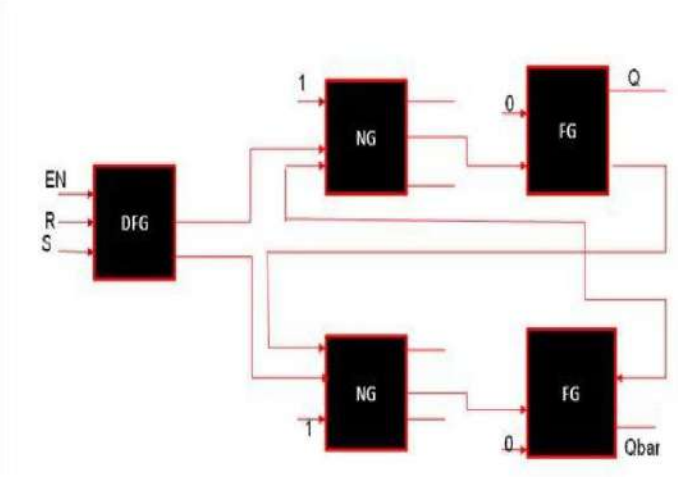


**Figure 1: Shows SR Flip-Flop using Reversible Gates**

The proposed SR Flip-flop contains 1 DFG , 2-NG gates & 2-FG gates. The characteristic equation of SR flip flop is $Q=S+R'Q$ . The SR flip-flop can be mapped by giving S, R and En inputs to the DFG gate.

**Table 1: Shows Number of gates used**

| Gate used to design SR flip-flop | Garbage Output | Number of Gates |
|---|---|---|
| Double Feynman Gate | 0 | 1 |
| New Gate | 4 | 2 |
| Feynman Gate | 0 | 2 |

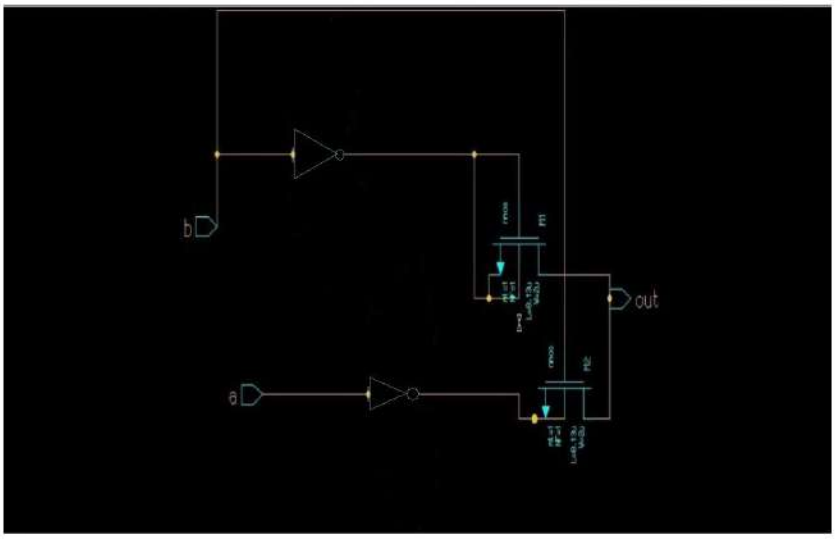


**Figure 2 : Shows NAND gate using Transmission Gate Logic**

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The proposed NAND gate comprises of two NMOS devices whereas NAND gate using conventional CMOS Logic consists of four MOS devices. By, reducing MOS devices in nand gate the transistor count gets reduced as well as in SR flip-flop. The transmission gate logic NAND gates are used to design the SR flip-flop and the designed SR flip flop is as shown in figure below. The inputs to the SR flip flop are S(set), R(Reset) and clock signal.

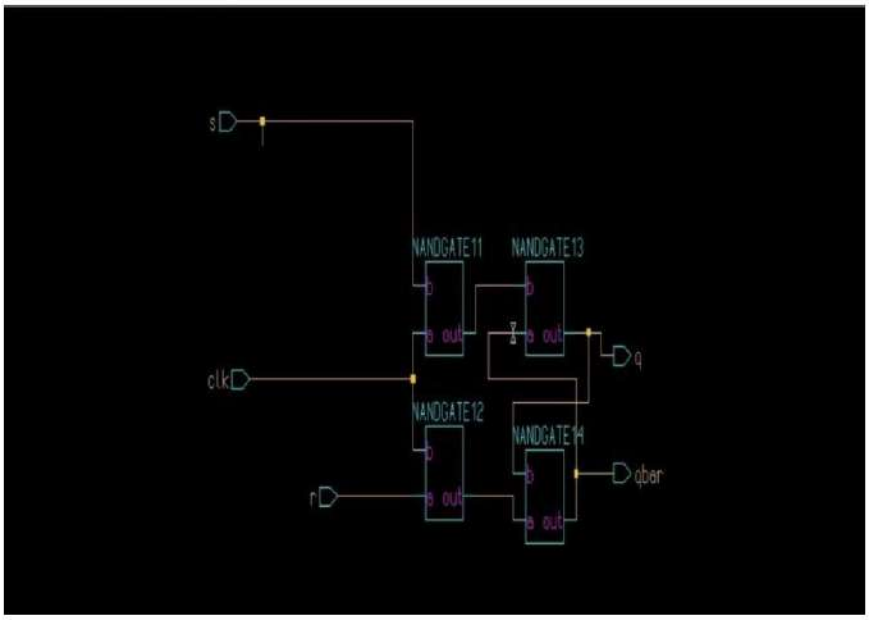


**Figure 3: Shows SR Flip-Flop using NAND gates**

**D-Flip-Flop:**

The D flip flop can be constructed using SR Flip-flop by applying inverted inputs to S and R inputs. The inputs to D flip flop are D and CLK and the output is next state. Transmission gate logic is also used to design D flip flop.SR can be used to construct D flip flop. The D flip flop constructed by using reversible logic is shown in figure below.

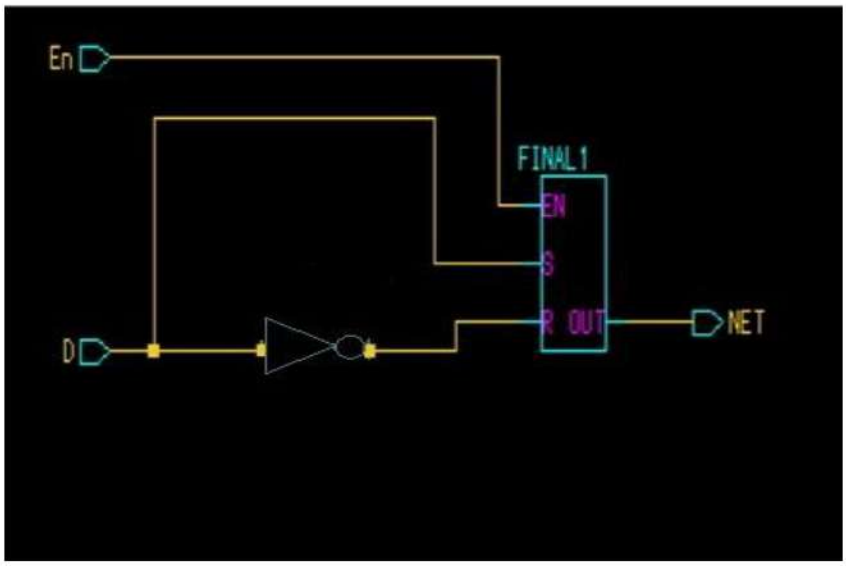


**Figure 4: Shows D flip-flop using Reversible Logic**

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The D flip flop constructed by using transmission gate logic is shown in figure below:

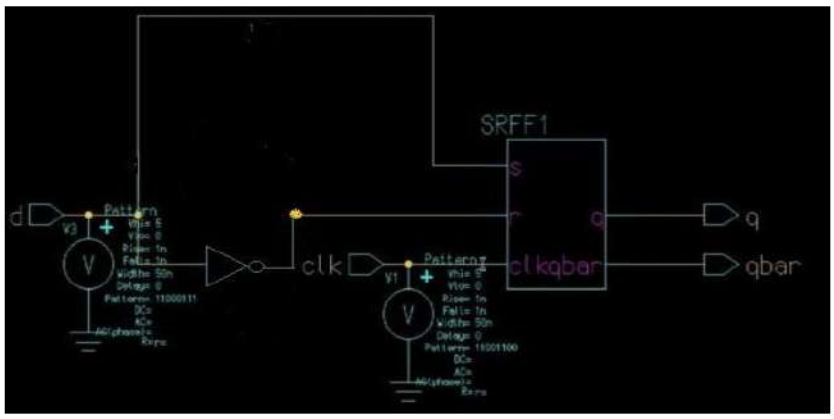


**Figure 5: Shows D Flip-Flop using transmission gate logic**

## III.RESULTS

To check the power dissipation of the proposed flip-flops using reversible logic and transmission gate logic are developed. The waveform representation of power dissipation of proposed flip-flops are presented in figure-6 to figure-14 which illustrates the waveforms of proposed models implemented using reversible logic and transmission gate logic.

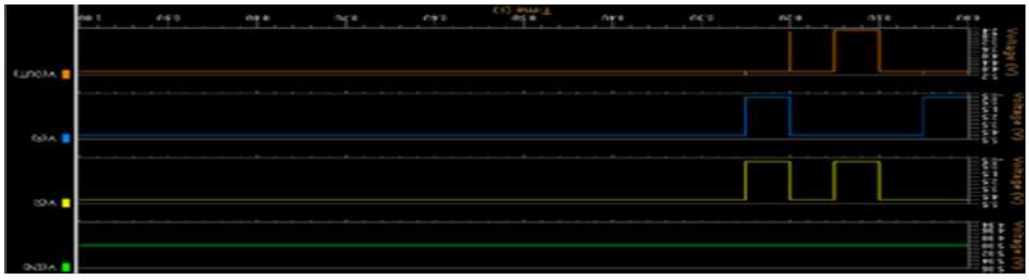

**Figure 6: Shows Results of Reversible SR Flip-Flop**

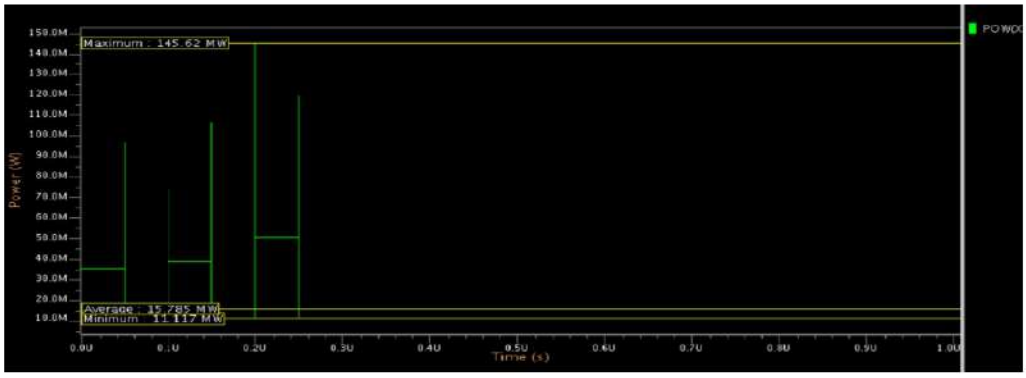


**Figure 7: Shows Power dissipation of Reversible SR Flip-Flop**

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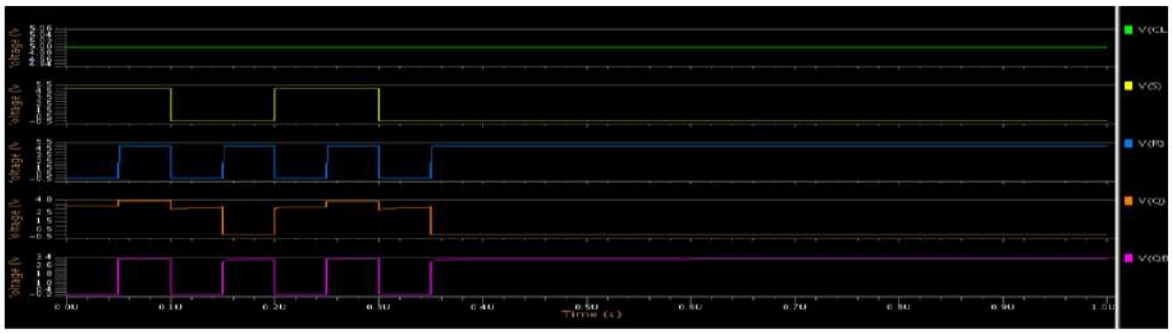

**Figure 8: Shows Results of Transmission Gate Logic SR Flip-Flop**

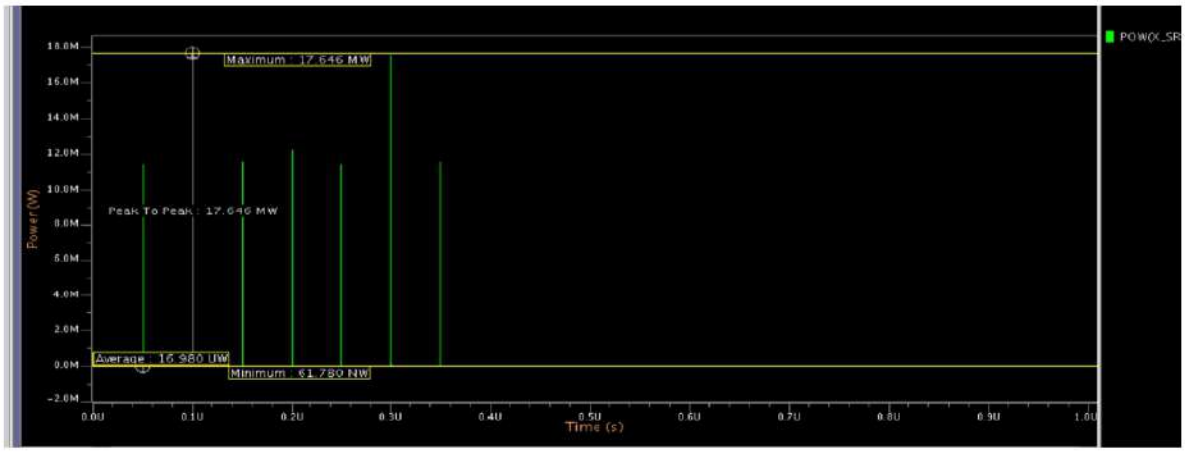


**Figure 9: Shows Power dissipation of Transmission Gate Logic SR Flip Flop**

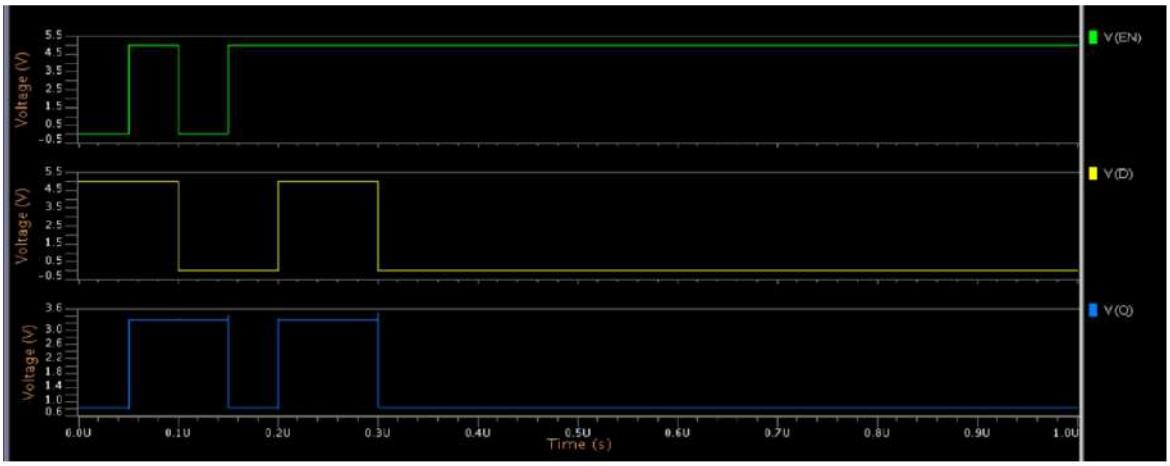


**Figure 10: Shows Power dissipation of Transmission Gate Logic SR Flip Flop**

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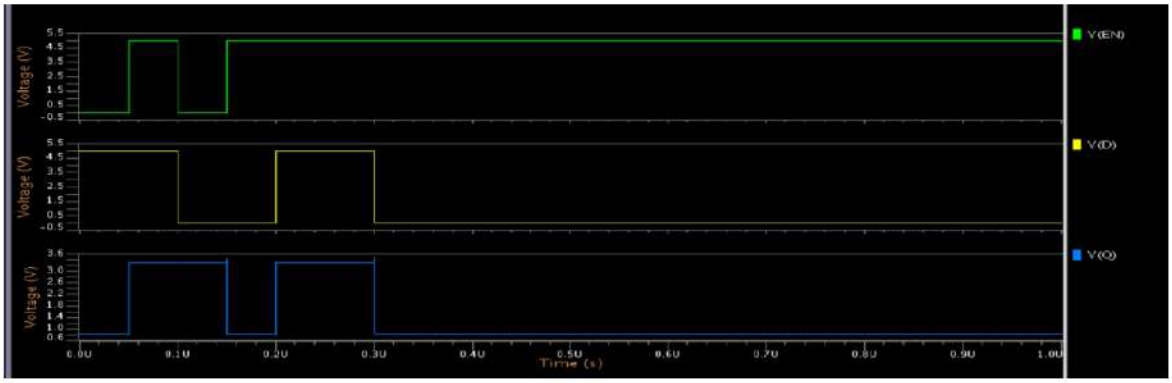


**Figure 11: Shows Results of Reversible D Flip Flop**

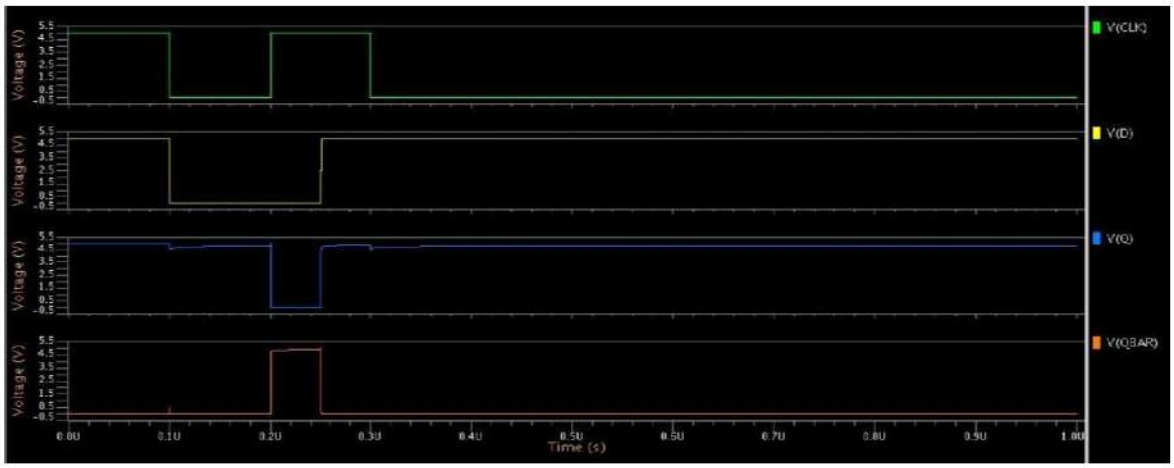


**Figure 11: Shows Power dissipation of D Flip-Flop**

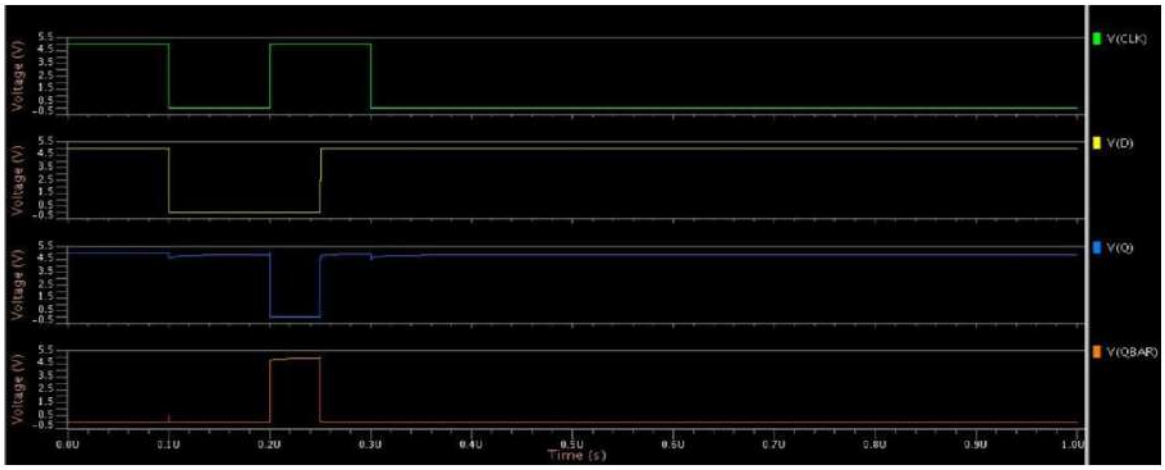


**Figure 12: Shows Results of D flip flop using transmission gate logic**

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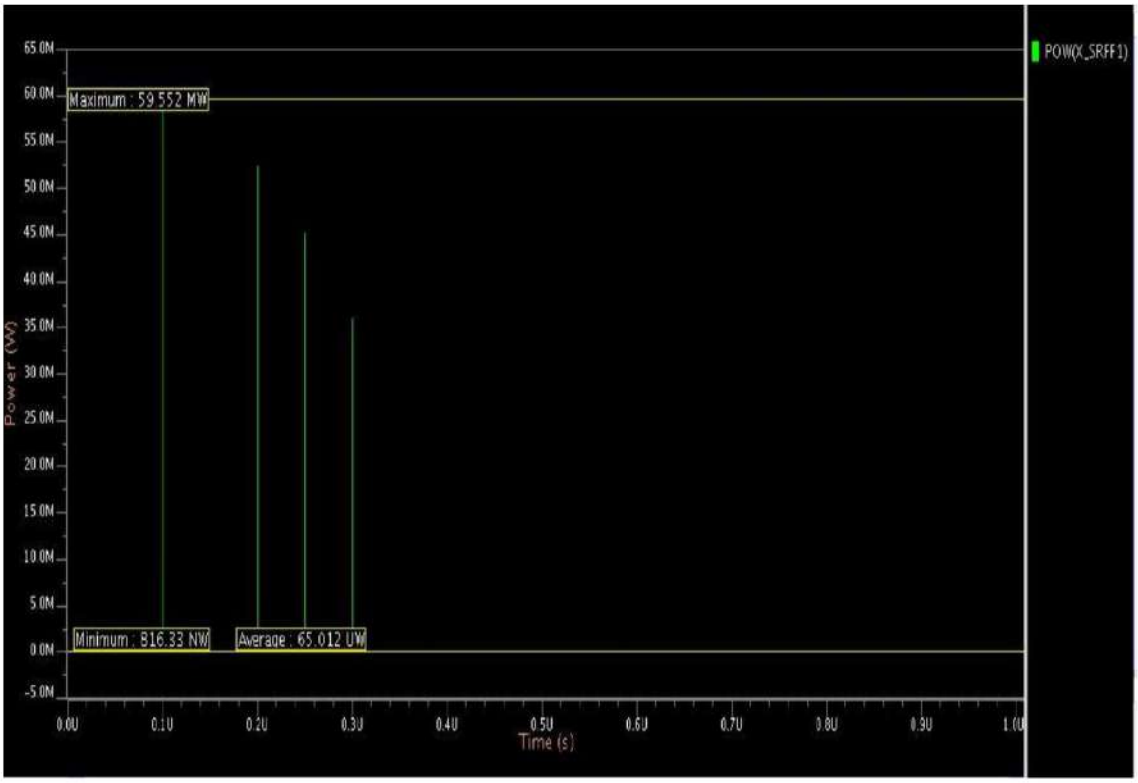


**Figure 13: Shows Power dissipation by Transmission Gate D flip-flop**

## IV.CONCLUSION

In this project we completely studied the basic existing reversible gates and their truth tables are verified by simulation and designed reversible SR & D flip flops by using the various basic reversible gates. The proposed reversible logic flip flops contains reduced number of gates, garbage outputs and constant inputs.

Reversible latches are the main memory blocks for the upcoming quantum devices. Along with reversible logic, transmission gate logic are simulated and the SR flip flop and D flip flop using NAND gates is designed. Both the proposed designs are simulated and the tested with various input values. The extensions in the digital design developments using reversible logic circuits which are helpful in quantum computing, DNA computing, digital signal processing, low power CMOS and computer graphics.

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